Solutions - Midterm Exam

(February 16th @ 5:30 pm)

Presentation and clarity are very important! Show your procedure!

Problem 1 (24 pts)

a) Complete the following table. The decimal numbers are unsigned: (5 pts.)

Decimal	BCD	Binary	Reflective Gray Code
31	00110001	11111	10000
33	00110011	100001	110001
247	001001000111	11110111	10001100

b) Complete the following table. The decimal numbers are signed. Use the fewest number of bits in each case: (15 pts.)

	REPRESENTATION		
Decimal	**Sign-and-magnitude**	**1's complement**	**2's complement**
-10	11010	10101	10110
-15	11111	10000	10001
13	01101	01101	01101
-11	11011	10100	10101
-31	111111	100000	100001
-25	111001	100110	100111

c) Convert the following decimal numbers to their 2's complement representations. (4 pts)

✓ -31.5

+31.5 = 011111.1 ⇒ -31.5 = 100000.1

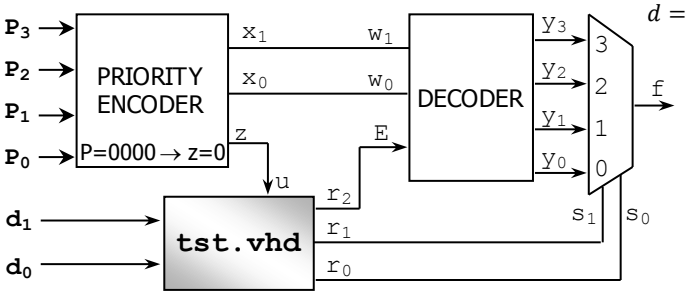
✓ 25.25

+25.25 = 011001.01

Problem 2 (18 pts)

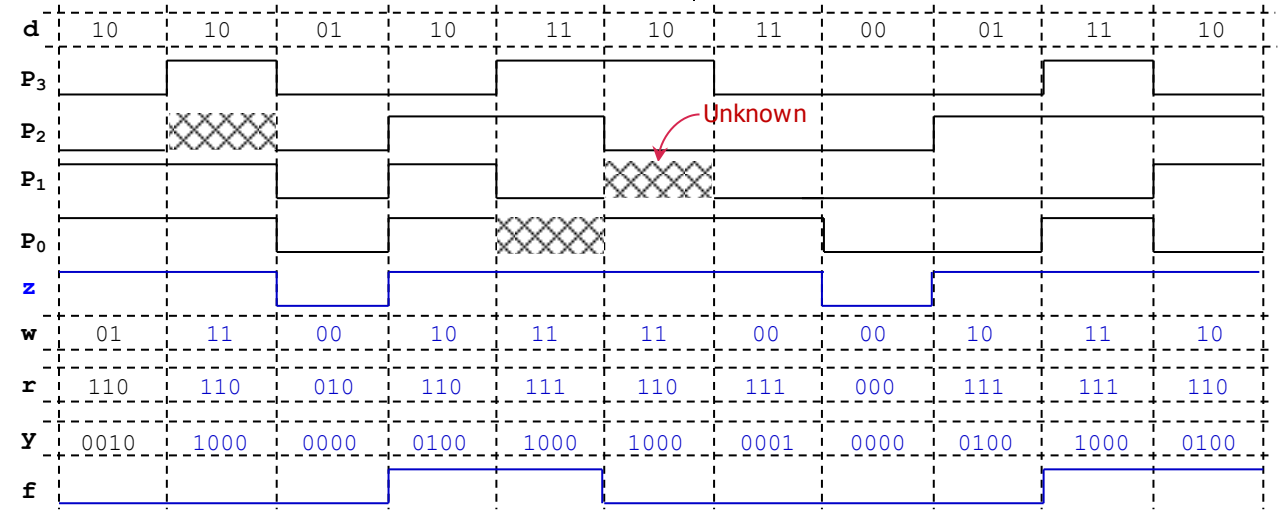
- Complete the timing diagram of the following circuit. The VHDL code (tst.vhd) corresponds to the shaded circuit.

$d = d_1d_0$, $w = w_1w_0$, $r = r_2r_1r_0$, $y = y_3y_2y_1y_0$



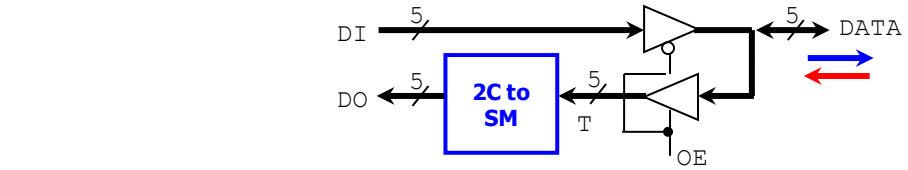

```
library ieee;
use ieee.std_logic_1164.all;
entity tst is
  port (d: in std_logic_vector(1 downto 0);
        r: out std_logic_vector(2 downto 0);
        u: in std_logic);
end tst;
```

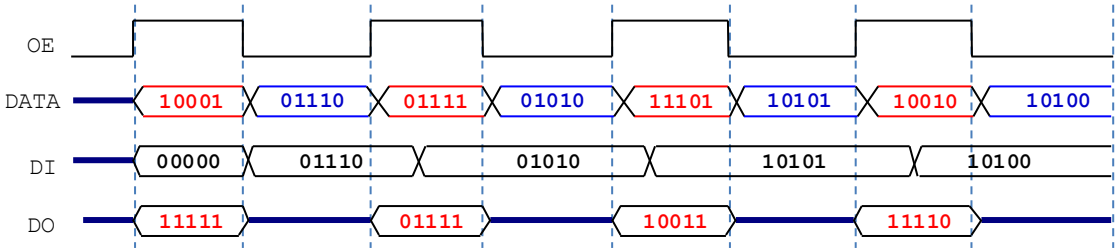
```
architecture bhv of tst is

begin

  process (d, u)
  begin

     r <= "11"&d(0);
     if u = '0' then
        r <= d&'0';
     end if;

  end process;

end bhv;
```



PROBLEM 3 (12 PTS)

- Complete the timing diagram (signals *DO* and *DATA*) of the following circuit. The circuit in the blue box treats the input T as a 5-bit signed (2C) number and converts it to the sign-and-magnitude representation with 5 bits.
  - ✓ Example: if T = 10110, then DO = 11010.



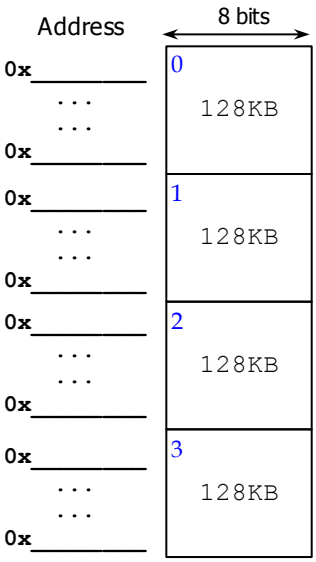


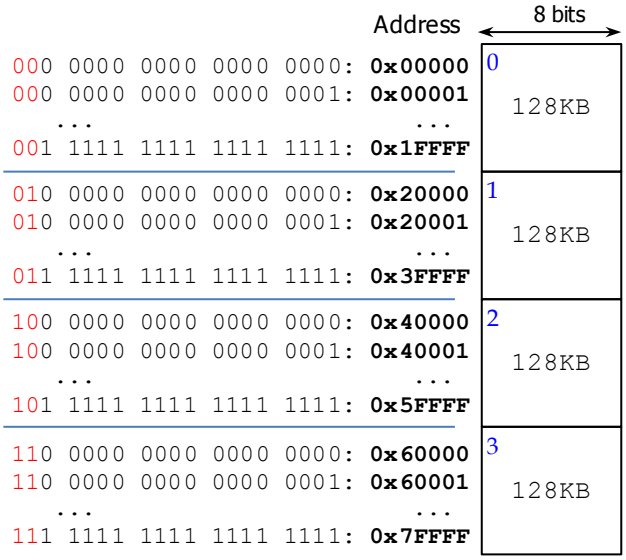
PROBLEM 4 (11 PTS)

- A microprocessor has a memory space of 512 KB. Each memory address occupies one byte.
  a) What is the address bus size (number of bits of the address) of this microprocessor?
  Since 512 KB = 2^{19} bytes, the address bus size is 19 bits.

  b) What is the range (lowest to highest, in hexadecimal) of the memory space for this microprocessor?
  With 19 bits, the address range is `0x0000` to `0x7FFFF`.

  c) The figure to the right shows four memory chips that are placed in the given positions:
  - ✓ Complete the address ranges (lowest to highest, in hexadecimal) for each of the memory chips.





PROBLEM 5 (18 PTS)

a) Perform the binary unsigned subtraction of these unsigned integers. Use the fewest number of bits n to represent both operators. Indicate every borrow from b_0 to b_n. Determine whether we need to keep borrowing from a higher byte. (6 pts)
   - ✓ 31 – 37

Borrow out! → b_6=1 b_5=0 b_4=0 b_3=0 b_2=0 b_1=0 b_0=0

```
31 = 0x1F =  0 1 1 1 1 1 -
37 = 0x25 =  1 0 0 1 0 1
-------------------------
             1 1 1 0 1 0
```

b) Perform the binary operation of these numbers, where numbers are represented in 2's complement. Indicate every carry from c_0 to c_n. Use the fewest number of bits to represent the summands and the result so that overflow is avoided. (8 pts)

✓ 31 – 37

n = 7 bits

c_7=0 c_6=0 c_5=1 c_4=1 c_3=1 c_2=1 c_1=1 c_0=0

$c_7 \oplus c_6 = 0$
No Overflow

```
31 =  0  0  1  1  1  1  1  +
-37 =  1  0  1  1  0  1  1
-----------------------------
-6 =  1  1  1  1  0  1  0
```

$31 - 37 = -6 \in [-2^6, 2^6-1] \rightarrow$ no overflow

c) Perform binary multiplication of the following numbers that are represented in 2's complement arithmetic. (4 pts)

✓ -11 x 7

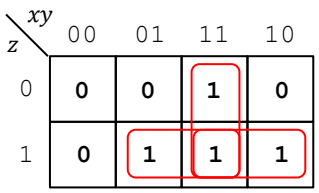
```
1 0 1 0 1 x          1 0 1 1 x
0 0 1 1 1            0 1 1 1
                     -------
                       1 0 1 1
                     1 0 1 1
                   1 0 1 1
                 0 0 0 0
                 -------
               0 1 0 0 1 1 0 1
                     ↓
               1 0 1 1 0 0 1 1
```

PROBLEM 6 (17 PTS)

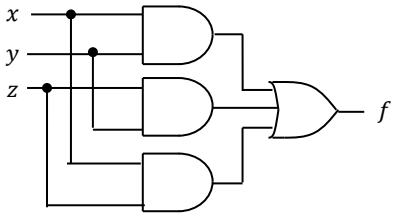
- A 3-input majority gate has an output value f that is 1 if there are more 1's than 0's on its inputs. The output f is 0 otherwise.

a) Provide the simplified expression for f and sketch this circuit using logic gates. (5 pts)

x	y	z	f
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1



$f = xy + yz + xz$



b) Implement the previous circuit using ONLY 2-to-1 MUXs (AND, OR, NOT, XOR gates are not allowed). (12 pts)

$f(x,y,z) = \bar{x}f(0,y,z) + xf(1,y,z) = \bar{x}(yz) + x(y + yz + z) = \bar{x}g(y,z) + xh(y,z)$

$g(y,z) = \bar{y}g(0,z) + yg(1,z) = \bar{y}(0) + y(z)$
$h(y,z) = \bar{y}h(0,z) + yh(1,z) = \bar{y}(z) + y(1)$